In the Claims

CLAIMS

1. (Currently amended) A method of forming a capacitor comprising the following steps:

~~forming a capacitor plate,~~ forming a capacitor plate comprising:

forming a solid mass of silicon material within an opening formed over a doped region of a silicon substrate, the mass comprising only two forms of silicon, the mass including undoped silicon in physical contact with the doped region; and

substantially selectively forming rugged polysilicon from one of the forms of silicon and not from another of the forms of silicon; and

forming a cell plate proximate the rugged polysilicon.

2. (Original) The method of claim 1 wherein the two forms of silicon comprise doped silicon and undoped silicon.

3. (Original) The method of claim 2 wherein the doped silicon comprises a dopant concentration of at least 5×10^{18} atoms/cm^3 and wherein the undoped silicon comprises a dopant concentration of less than 5×10^{18} atoms/cm^3.

4. (Original) The method of claim 2 wherein the doped silicon comprises a dopant concentration of at least 1 x 10^{19} atoms/cm^3 and wherein the undoped silicon comprises a dopant concentration of less than or equal to 1 x 10^{18} atoms/cm^3.

5. (Currently amended) A method of forming a capacitor comprising the following steps:

forming a solid mass of silicon material over a doped diffusion region of a silicon substrate, the mass comprising a solid core of doped silicon substantially surrounded by undoped silicon leaving exposed doped silicon and exposed undoped silicon, and ~~including~~ the mass further comprising a portion of the undoped silicon in contact with the doped diffusion region;

substantially selectively forming rugged polysilicon from the exposed undoped silicon and not from the exposed doped silicon; and

forming a cell plate proximate the rugged polysilicon.

6. (Currently amended) The method of claim 5 wherein the step of forming a mass of silicon material comprises forming ~~a layer~~ the solid core of doped silicon ~~between two layers~~ within a cylinder of undoped silicon.

7. (Previously presented) The method of claim 5, further comprising conductively doping the undoped silicon after forming the rugged polysilicon.

8. (Previously presented) The method of claim 5, further comprising, after forming the rugged polysilicon, out-diffusing impurity from the doped silicon into the undoped silicon to conductively dope the undoped silicon.

9. (Original) The method of claim 5 wherein the step of forming the mass comprises forming the exposed undoped silicon to be substantially amorphous.

10. (Original) The method of claim 5 wherein the step of forming the mass comprises forming the exposed doped silicon to be substantially polycrystalline.

11. (Previously presented) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region of a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming two forms of silicon within and filling the opening, the two forms of silicon including undoped silicon in contact with the doped region;

exposing the two forms of silicon to common subsequent processing conditions which substantially selectively form rugged polysilicon from one of the exposed two forms of silicon and not from another of the exposed two forms of silicon; and

forming a cell plate proximate the rugged polysilicon.

12. (Original) The method of claim 11 wherein the two forms of silicon comprise doped silicon and undoped silicon.

13. (Currently amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region on a semiconductor wafer substrate;

forming an opening through the insulative layer to the doped region;

forming silicon material within the opening, the silicon material comprising doped silicon and undoped silicon and defining a capacitor storage node, a portion of the undoped silicon being in physical contact with the doped region;

removing a portion of the insulative layer to expose ~~a~~ an outer sidewall surface of the storage node, the exposed outer sidewall surface comprising undoped silicon;

forming HSG from the undoped silicon of the exposed outer sidewall surface, the exposed outer sidewall surface comprising an only portion of the storage node which comprises HSG; and

forming a cell plate proximate the storage node.

14. (Original) The method of claim 13 wherein the doped silicon comprises polysilicon and the undoped silicon comprises substantially amorphous silicon.

15. (Currently amended) The method of claim 13 wherein the step of forming the silicon material comprises forming a ~~layer~~ solid core of the doped silicon ~~between two layers of~~ surrounded by the undoped silicon.

16. (Currently amended) The method of claim 13 wherein the step of forming the silicon material comprises forming a ~~layer~~ solid core of the doped silicon as polysilicon ~~between two layers of~~ surrounded by the undoped silicon, the undoped silicon comprising undoped substantially amorphous silicon.

17. (Currently amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region on a semiconductor substrate;

forming an opening through only the insulative layer to the doped region;

forming an undoped silicon layer within the opening to narrow the opening, a portion of the undoped silicon contacting the doped region;

forming a doped silicon layer within the narrowed opening, the undoped silicon layer and doped silicon layer together defining substantially an entirety of structural material for a capacitor storage node; and

forming a cell plate proximate the storage node.

18. (Original) The method of claim 17 wherein the undoped silicon layer comprises substantially amorphous silicon.

19. (Original) The method of claim 17 wherein the doped silicon layer comprises polysilicon.

20. (Original) The method of claim 17 further comprising:

removing a portion of the insulative layer to expose a sidewall surface of the storage node comprising the undoped silicon layer; and

forming rugged polysilicon from the exposed sidewall surface.

21. (Original) The method of claim 17 further comprising:

exposing a surface of the capacitor storage node comprising undoped silicon;

exposing a surface of the capacitor storage node comprising doped silicon; and

substantially selectively forming HSG polysilicon from the exposed capacitor storage node surface comprising undoped silicon and not from the exposed capacitor storage node surface comprising doped silicon.

22. (Original) The method of claim 21 wherein the formation of the rugged polysilicon comprises:

in situ HF cleaning of the exposed sidewall surface;

seeding the exposed sidewall surface with polysilicon; and

annealing the seeded sidewall surface at about 560°C for about 20 minutes.

23. (Original) The method of claim 21 wherein the formation of the rugged polysilicon comprises:

in situ HF cleaning of the exposed sidewall surface;

seeding the exposed sidewall surface with polysilicon;

annealing the seeded sidewall surface at about 560°C for about 20 minutes; and

a polysilicon etch after the annealing to remove any monolayers of silicon.

24. (Previously presented) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming a first undoped silicon layer within the opening to narrow the opening, a portion of the undoped silicon layer contacting the doped region;

forming a doped silicon layer within the narrowed opening to further narrow the opening;

forming a second undoped silicon layer within the further narrowed opening; the first undoped silicon layer, second undoped silicon layer and doped silicon layer together defining a capacitor storage node;

removing a portion of the insulative layer to expose a sidewall surface of the storage node comprising the first undoped silicon layer;

forming rugged polysilicon on only the exposed sidewall surface; and

forming a cell plate proximate the storage node.

25. (Original) The method of claim 24 further comprising:

exposing a surface of the capacitor storage node comprising the second undoped silicon layer;

exposing a surface of the capacitor storage node comprising the doped silicon layer; and

substantially selectively forming HSG polysilicon from the exposed capacitor storage node surface comprising undoped silicon and not from the exposed capacitor storage node surface comprising doped silicon.

Claims 26-43 (Canceled).

44. (Previously presented) The method of claim 1, wherein forming a cell plate comprises forming a capacitor dielectric layer and a complementary capacitor plate proximate the rugged polysilicon.

45. (Previously presented) The method of claim 5, wherein forming a cell plate comprises forming a capacitor dielectric layer and a complementary capacitor plate proximate the rugged polysilicon and doped silicon.

46. (Previously presented) The method of claim 11, wherein forming a cell plate comprises:

forming a dielectric layer proximate the storage node; and

forming a cell plate layer proximate the dielectric layer.

47. (Previously presented) The method of claim 13, wherein forming a cell plate comprises:

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

48. (Previously presented) The method of claim 17, wherein forming a cell plate comprises:

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

49. (Previously presented) The method of claim 24, wherein forming a cell plate comprises:

forming a dielectric layer proximate the storage node; and

forming a cell plate layer proximate the dielectric layer.

50. (Previously presented) A method of forming a capacitor comprising:

forming an insulative layer over a doped region formed on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

filling the opening with silicon material, the silicon material comprising doped silicon and undoped silicon and defining a capacitor storage node;

removing a portion of the insulative layer to expose a sidewall surface of the storage node, the exposed sidewall surface comprising undoped silicon;

forming HSG from the undoped silicon of the exposed sidewall surface; and

forming a cell plate proximate the storage node.

51. (Previously presented) The method of claim 50, wherein forming a cell plate comprises:

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

52. (Previously presented) The method of claim 50 wherein the doped silicon comprises polysilicon and the undoped silicon comprises substantially amorphous silicon.

53. (Previously presented) The method of claim 50 wherein forming the silicon material comprises forming a layer of doped silicon inside a layer of undoped silicon.

54. (Previously presented) The method of claim 50 wherein filling the opening with silicon material comprises forming a layer of doped polysilicon within a layer of undoped substantially amorphous silicon.

55. (Previously presented) A method of forming a capacitor comprising:

forming an insulative layer over a doped region formed on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming an undoped silicon layer within the opening to narrow the opening;

filling the narrowed opening with a doped silicon layer, the undoped silicon layer and doped silicon layer together defining a capacitor storage node; and

forming a cell plate proximate the storage node.

56. (Currently amended) The method of claim 55, wherein forming a cell plate comprises:

forming a capacitor dielectric layer proximate the storage node; and

forming a complementary capacitor plate proximate the capacitor dielectric layer.

57. (Previously presented) The method of claim 55 further comprising:

exposing a surface of the capacitor storage node comprising undoped silicon;

exposing a surface of the capacitor storage node comprising doped silicon; and

substantially selectively forming HSG polysilicon from the exposed capacitor storage node surface comprising undoped silicon and not from the exposed capacitor storage node surface comprising doped silicon.

58. (Previously presented) The method of claim 57 wherein forming HSG polysilicon comprises:

in situ HF cleaning of exposed doped and undoped silicon surfaces;

seeding the exposed undoped silicon surface with polysilicon; and

annealing the seeded surface at about 560°C for about 20 minutes.

59. (Previously presented) The method of claim 57 wherein forming HSG polysilicon comprises:

in situ HF cleaning of the exposed doped and undoped silicon surfaces;

seeding the exposed undoped silicon surface with polysilicon;

annealing the seeded surface at about 560°C for about 20 minutes; and

a polysilicon etch after the annealing to remove any monolayers of silicon.